Customer No.: 31561
Application No.: 10/711,509
Docket No.: 12405-US-PA-0P

REMARKS

Present Status of the Application

The Office Action has rejected claims 1-2, 8-10, 20 and 25 under 35 U.S.C. 102(e) as being anticipated by Lee et al. US Patent No. 6,737,305 and claims 3-7, 21-24, 26 and 27 under U.S.C. 103(a) as being unpatentable over Lee in view of Yang (US Publication 2002/0102781 A1).

Applicants have amended claims 1 and 19 to more clearly define the present invention. After entry of the foregoing amendments, claims 1-10 and 19-27 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicants respectfully traverse the 102(e) rejection of claims 1-2, 8-10, 20 and 25 because Lee et al. (US-6,737,305 B2, Lee hereinafter) does not teach every element recited in these claims.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is contained in the .... claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

The present invention is in general related a manufacturing method of a thin film transistor (TFT) as claims 1 and 19 recite:

> Claim 1. A manufacturing method of a thin film transistor (TFT), comprising:
> forming a gate over a substrate;

forming an inter-gate dielectric layer over the substrate covering the gate;

forming a channel layer over a portion of the inter-gate dielectric layer at least over the gate, wherein the channel layer is a lightly doped amorphous silicon layer; and

forming source/drain regions over the channel layer, wherein the source/drain regions are separated by a distance, ***and the lightly doped amorphous silicon layer between the source region and the drain region is a channel region***.

Claim 19. A manufacturing method of a thin film transistor (TFT), comprising:

forming a gate over a substrate;

forming an inter-gate dielectric layer over the substrate covering the gate;

forming a channel layer over a portion of the inter-gate dielectric layer at least over the gate, wherein the channel layer comprises a lightly doped amorphous silicon layer;

forming an ohmic contact layer over the channel layer; and

forming source/drain regions over the channel layer, wherein the source/drain regions are separated by a distance, ***and the lightly doped amorphous silicon layer between the source region and the drain region is a channel region***.

Lee fails to teach or suggest that the channel region between the source and drain regions of the TFT is/comprises a lightly doped amorphous layer. In Lee's reference, a first a-Si layer 106a and a second a-Si layer 106b are formed sequentially, and a N+Mixed a-Si layer 106c is subsequently formed on the surface of the second a-Si layer 106b (col. 5, lines 5-18). In particular, the first a-Si layer 106a is formed by using SiH_4/H_2 (col. 5, lines 41-54). The second a-Si layer 106b is formed by using SiH_4/H_2 (col. 5, line 65- col. 6, line 11). In other words, the first and second a-Si layers 106a, 106b are non-doped amorphous silicon layer. After that, the three layers 106a, 106b, 106c are patterned (Fig. 4D). Then, a source/drain 108 is formed. In the meanwhile, the N+Mixed a-Si layer 106c between the source and the drain is removed. The remained N+Mixed a-Si layer 106c is between the second a-Si layer 106b and the source/drain 108. Thus, the channel region between the source and the drain is composed of the second a-Si layer 106b and the first a-Si layer 106a

that are non-doped amorphous silicon layers. Hence, Lee does not teach or suggest that the channel region between the source and the drain is/comprises a lightly doped amorphous layer. Lee dose not teach every element in claims 1 and 19.

In particular, the channel region between the source and the drain is/comprises a lightly doped amorphous layer as claims 1 and 19 recite can overcome the problem of a-Si channel having low carrier mobility that is long-left need, and the manufacturing method of claims 1 and 19 does not need additional high cost processes.

For at least the foregoing reasons, Applicants respectfully submit that independent claims 1 and 19 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2, 8-10, 20 and 25 patently define over the prior art as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claims.

Applicants respectfully traverse the rejection of claims 3-7, 21-24, 26 and 27 under 103(a) as being unpatentable over Lee in view of Yang et al. (US Publication, hereinafter Yang) because a prima facie case of obviousness has not been established by the Office Action.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner

resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

Applicants submit that, as disclosed above, Lee fails to teach or suggest each and every element of claims 1, 19 from which claims 3-7, 21-24, 26 and 27 depend. In Yang's reference, the portion A (Fig. 2D) of the doped polysilicon island 156b between the source and drain electrodes 160, 162 is removed. Thus, the channel region between the source 160 and the drain 162 is the intrinsic polysilicon layer 154a (paragraph [0040-0041]). Therefore, Yang also fails to teach that the channel region between the source and the drain is a lightly doped amorphous silicon layer. Yang cannot cure the deficiencies of Lee. Therefore, independent claims 1 and 19 are patentable over Lee and Yang. For at the least the same reasons, their dependent claims 3-7, 21-24, 26 and 27 are also be patentable.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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